WHAT IS CLAIMED IS:

1. A semiconductor memory device which comprises an insulating film formed on the principal plane of a semiconductor substrate, a first electrode formed on said insulating film, a second electrode capable of being controlled independently of said first electrode which is formed on the region including said first electrode, with an insulating film interposed therebetween, a diffusion layer formed on the surface of said semiconductor substrate a prescribed distance away from said first electrode, a charge storage region to hold charge, with its periphery surrounded by an insulating film in the vicinity of the semiconductor surface between said first electrode and said diffusion layer, and an inversion layer region to be formed on said semiconductor surface upon application of a voltage to said first electrode, said charge storage region being controlled by said second electrode such that information is stored by utilizing the fact that conductance between said diffusion layer and said inversion layer region changes according to the amount of charge stored in said charge storage region.

2. A semiconductor memory device which comprises a well region of the first conduction type which is formed in a semiconductor substrate, a first and second diffusion

layers of the second conduction type which are formed in said well region, an insulating film formed on the surface of the semiconductor substrate between said first and second insulating layers, a first electrode formed on said insulating film, a second electrode capable of being controlled independently of said first electrode, a first charge storage region to hold charge, with its periphery surrounded by an insulating film in the vicinity of the semiconductor surface between said first electrode and said first diffusion layer, a second charge storage region to hold charge, with its periphery surrounded by an insulating film in the vicinity of the semiconductor surface between said first electrode and said second diffusion layer, an inversion layer region to be formed on said semiconductor surface upon application of a voltage to said first electrode, and a third diffusion layer of the second conduction type which is formed such that it overlaps with one end of said inversion layer region, the potential of said first charge storage region and said second charge storage region being controlled by said second electrode such that information is stored by utilizing the fact that conductance between said first diffusion layer and said third diffusion layer changes according to the amount of charge stored in said first charge storage region and information is stored by utilizing the fact that conductance between said second

diffusion layer and said third diffusion layer changes according to the amount of charge stored in said second charge storage region.

3. The semiconductor memory device as defined in Claim 2, wherein the potential of said first diffusion layer is set at potential A, the potential of said second diffusion layer is set at potential B which is higher than said potential A, and the potential of said first electrode is set at potential C which is lower than said potential B, thereby causing the hot electrons, which occur on the surface of the semiconductor substrate between said first electrode and said second diffusion layer, to be injected into said second charge storage region.

4. The semiconductor memory device as defined in Claim 2, wherein the potential of said second diffusion layer is set at potential A, the potential of said first diffusion layer is set at potential B which is higher than said potential A, and the potential of said first electrode is set at potential C which is lower than said potential B, thereby causing the hot electrons, which occur on the surface of the semiconductor substrate between said first electrode and said first diffusion layer, to be injected into said first charge storage region.

5. The semiconductor memory device as defined in Claim 2, wherein the potential of said second electrode is set at potential A, the potential of said first diffusion layer is set at potential B, the potential of said second diffusion layer is set at potential C which is higher than said potential B and then brought into a floating state by disconnecting the power source, and the potential of said first electrode is set at potential D which is lower than said potential C, thereby causing the hot electrons, which occur on the surface of the semiconductor substrate between said first electrode and said second diffusion layer, to be injected into said second charge storage region.

6. A semiconductor memory device which comprises a first and second electrodes parallel to each other in a first direction which are formed on a semiconductor substrate, a third electrode to control the potential of the surface of the semiconductor substrate between said first and said second electrodes which is formed in a second direction perpendicular to said first direction, and a charge storage region to hold charge, with its periphery surrounded by an insulating film, which is formed between said first and second electrodes, the surface of the semiconductor substrate between said first electrode and said second

electrode being constructed of a region having the first conduction type such that information is stored by utilizing the fact that conductance of the surface of said semiconductor substrate in the vicinity of said charge storage region changes according to the amount of charge stored in said charge storage region.

7. A semiconductor memory device which comprises a first and second electrodes parallel to each other in a first direction which are formed on a semiconductor substrate, a third electrode to control the potential of the surface of the semiconductor substrate between said first and said second electrodes which is formed in a second direction perpendicular to said first direction, and a charge storage region to hold charge, with its periphery surrounded by an insulating film, which is formed between said first and second electrodes, a first inversion layer being formed in the vicinity of the surface of said semiconductor substrate upon application of a voltage to said first electrode and a second inversion layer being formed in the vicinity of the surface of said semiconductor substrate upon application of a voltage to said second electrode such that information is stored by utilizing the fact that conductance of the surface of said semiconductor substrate between said first inversion layer and said second inversion layer changes

according to the amount of charge stored in said charge storage region.

8. The semiconductor memory device as defined in Claim 1, wherein information of 2 bits or more is stored in the charge storage regions each holding charge by changing the amount of charge injected into the charge storage region.

9. A semiconductor memory device which has at least 8 electrodes (a first to an eighth electrodes) parallel to one another arranged in a first direction, a plurality of electrodes arranged in a second direction perpendicular to said first direction, said first to said fourth electrodes being connected respectively to said fifth to said eighth electrodes, at least one of said first to said fourth electrodes being set at a prescribed potential in the operation of writing information in the element formed on said semiconductor substrate, the surface of said semiconductor substrate in the vicinity of the electrode which has been set at said prescribed potential being in a non-conduction state so that the element is electrically isolated.

10. A semiconductor memory device which comprises a first and second electrodes parallel to each other in a first

direction which are formed on a semiconductor substrate, a third electrode to control the potential of the surface of the semiconductor substrate between said first and said second electrodes which is formed in a second direction perpendicular to said first direction, and a charge storage region to hold charge, with its periphery surrounded by an insulating film, which is formed between said first and said second electrodes, said first electrode being set at potential A so that a first inversion layer is formed in the vicinity of the surface of said semiconductor substrate, the potential of said first inversion layer being set at potential B which is lower than said potential A, the potential of said second electrode being set at potential C so that a second inversion layer is formed in the vicinity of the surface of said semiconductor substrate, the potential of said inversion layer being set at potential D which is higher than said potential B and lower than said potential C, the potential of said third electrode being set at potential E which is higher than said potential D, thereby causing the hot electrons, which occur in the vicinity of said first electrode, to be injected into said first charge storage region.

11. A semiconductor memory device which comprises a first, second, and third electrodes parallel to one another in a

first direction which are formed on a semiconductor substrate, a fourth electrode to control the potential of the surface of the semiconductor substrate between said first and second electrodes and between said second and third electrodes which is formed in a second direction perpendicular to said first direction, a first charge storage region to hold charge, with its periphery surrounded by an insulating film, which is formed between said first and second electrodes, and a second charge storage region to hold charge, with its periphery surrounded by an insulating film, which is formed between said second and third electrodes, said first electrode being set at potential A so that a first inversion layer is formed in the vicinity of the surface of said semiconductor substrate, the potential of said first inversion layer being set at potential B which is lower than said potential A, the potential of said third electrode being set at potential C so that a second inversion layer is formed in the vicinity of the surface of said semiconductor substrate, the potential of said inversion layer being set at potential D which is higher than said potential B and lower than said potential C, the potential of said second electrode being set at potential E which is lower than said potential D, the potential of said fourth electrode being set at potential F which is higher than said potential D, thereby causing the

hot electrons, which occur on the surface of the semiconductor substrate between said second and third electrodes, to be injected into said second charge storage region.

12. A semiconductor memory device which comprises a first and second electrodes parallel to each other in a first direction which are formed on a semiconductor substrate, a third electrode to control the potential of the surface of the semiconductor substrate between said first and second electrodes which is formed in a second direction perpendicular to said first direction, a charge storage region to hold charge, with its periphery surrounded by an insulating film, which is formed between said first and second electrodes, a first and second inversion layer regions to be formed on said semiconductor surface upon application of a voltage to said first and second electrodes, and a first and second diffusion layers formed such that they overlap respectively with one end of said first and second inversion layer regions, the potential of said third electrode being set at potential A and the potential of said first electrode being set at potential B so that a first inversion layer is formed in the vicinity of the surface of said semiconductor substrate, the potential of said first inversion layer being set at

potential C which is lower than said potential B then brought into a floating state by disconnecting the power source, the potential of said second electrode being set at potential D which is lower than said potential A and B, and the potential of said second diffusion layer being set at potential E which is lower than said potential A, B, C, and D, thereby causing the hot electrons, which occur in the vicinity of said second electrode, to be injected into said charge storage region.

13. A semiconductor memory device which is characterized in that the memory cell having the semiconductor memory device defined in Claim 12 possesses a power source circuit capable of changing the potential of said second electrode according to the address information of said memory cell at the time of writing.

14. A semiconductor memory device which comprises a first, second, and third electrodes parallel to one another in a first direction which are formed on a semiconductor substrate, a fourth electrode to control the potential of the surface of the semiconductor substrate between said first and second electrodes and between said second and third electrodes which is formed in a second direction perpendicular to said first direction, a first charge

storage region to hold charge, with its periphery surrounded by an insulating film, which is formed between said first and second electrodes, and a second charge storage region to hold charge, with its periphery surrounded by an insulating film, which is formed between said second and third electrodes, a first and second inversion layer regions to be formed on said semiconductor surface upon application of a voltage to said first and second electrodes, and a first and second diffusion layers formed such that they overlap respectively with one end of said first and second inversion layer regions, the potential of said first electrode being set at potential A so that a first inversion layer is formed in the neighboring semiconductor surface, the potential of said first inversion layer being set at potential B which is lower than said potential A, the potential of said third electrode being set at potential C so that a second inversion layer is formed in the vicinity of the semiconductor surface, the potential of said second inversion layer being set at potential D which is higher than said potential B and lower than said potential C then brought into a floating state by disconnecting the power source, the potential of said fourth electrode being set at potential E which is higher than said potential D, and the potential of said second electrode being set at potential F which is lower than said potential A, C, and E, thereby causing the hot

electrons, which occur on the surface of the semiconductor substrate between said second and third electrodes, to be injected into said second charge storage region.

15. A semiconductor memory device having a plurality of nonvolatile memory cells, which is characterized in that the sub-bit lines of said memory cells constitute said inversion layer and the writing or erasing in said memory cells is accomplished by discharging the charge stored in the capacity of said sub-bit lines through said memory cells and injecting the hot electrons that occur at this time into the floating gates in said memory cells.